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EXAMINER	
WILSON, YOLANDA L	
ART UNIT	**PAPER NUMBER**
2113	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/903,705	Applicant(s) GOODMAN ET AL.	
	Examiner Yolanda Wilson	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-38 are rejected under 35 U.S.C. 102(b) as being anticipated by Jardine et al. (USPN 5884018A). As per claim 1, Jardine et al. discloses at least a plurality of said processor nodes each having information of relative locations of said processor nodes on said multi-drop bus network; said plurality of processor nodes each independently testing access to at least one other of said processor nodes on said multi-drop bus network; upon said access testing by any of said plurality of testing processor nodes detecting a failure to access at least one of said other said processor nodes, said failure detecting processor node determining, from said information of relative locations, the processor node having failed access which is closest to said failure detecting processor node; and said failure detecting processor node storing an identification of said closest processor node having failed access in column 13, line 46 – column 14, line 21; lines 45-67.

3. As per claim 2, Jardine et al. discloses posting an identifier of said closet processor node having failed access at an associated error indicator local to said failure detecting processor node in column 13, line 46 – column 14, line 2.

4. As per claim 3, Jardine et al. discloses upon said access testing by any of said plurality of testing processor nodes detecting a failure to access all of said other processor nodes, said failure detecting processor node posting a special identifier at said associated local error indicator in column 22, lines 52-56.

5. As per claim 4, Jardine et al. discloses posting an error message representing said identifier to an error log; and subsequently accumulating said posted error messages of said plurality of processor nodes in column 13, line 46 – column 14, line 2.

6. As per claim 5, Jardine et al. discloses locking said posted identifier at said error indicator for a predetermined time-out period; and subsequent to expiration of said time-out period, deleting said posted identifier from said associated local error indicator in column 15, lines 15-41.

7. As per claim 6, Jardine et al. discloses locking said posted identifier at said error indicator; and responding to an operator initiated signal, deleting said posted identifier from said associated local error indicator in column 15, lines 15-41. The operator initiated signal is when the regroup message is sent.

8. As per claim 7, Jardine et al. discloses locking said posted identifier at said associated local error indicator; and said displaying processor node retesting said access, and, upon absence of an error during a predetermined number of said retests, deleting said posted identifier from said associated local error indicator in column 15, lines 10-41.

9. As per claim 8, Jardine et al. discloses said multi-drop bus network additionally comprises multiple processor nodes extending from a single drop of

said multi-drop bus network, upon said access failure detecting step detecting access failure of a plurality of said multiple processor nodes at said single drop, said step of determining said processor node having failed access additionally comprises determining, from said information of relative locations, said single drop having failed access which is closest to said failure detecting processor node, and selecting one of said multiple processor nodes at said single drop, said failure detecting processor node storing an identification of said selected processor node in column 13, line 46 – column 14, line 21; lines 45-67.

10. As per claim 9, Jardine et al. discloses one of said multiple processor nodes extending from said single drop of said multi-drop bus network is identified as having a higher priority than other processor nodes extending from said single drop, and wherein said selecting step comprises selecting said multiple processor node having said higher priority in column 13, line 46 – column 14, line 21; lines 45-67.

11. As per claim 10, Jardine et al. discloses a multi-drop bus network; processor nodes coupled by said multi-drop bus network, each of a plurality of said processor nodes having information providing relative locations of said processor nodes on said multi-drop bus network; said plurality of processor nodes each independently testing access to at least one other of said processor nodes on said multi-drop bus network; upon said access testing by any of said plurality of testing processor nodes detecting a failure to access at least one of said other said processor nodes, said failure detecting processor node determining, from said information of relative locations, the processor node

having failed access which is closest to said failure detecting processor node, and storing an identification of said closet processor node having failed access in column 13, line 46 – column 14, line 21; lines 45-67.

12. As per claim 11, Jardine et al. discloses additionally comprising a local error indicator associated with at least one of said plurality of processor nodes, said failure detecting processor node posting, at said local error indicator associated with said failure detecting processor node, an identifier of said closest processor node having failed access in column 13, line 46 – column 14, line 2.

13. As per claim 12, Jardine et al. discloses wherein said plurality of processor nodes, additionally, upon said access testing by any of said plurality of testing processor nodes detecting a failure to access all of said other processor nodes, said failure detecting processor node posting a special identifier at said associated local error indicator in column 22, lines 52-56.

14. As per claim 13, Jardine et al. discloses wherein each of said plurality of processor nodes additionally comprises an error log, and, upon detecting said access failure, posts an error message representing said identifier to said error log in column 13, line 46 – column 14, line 2.

15. As per claim 14, Jardine et al. discloses wherein at least one of said plurality of processor nodes additionally comprises a timer; and, upon detecting said access failure, locks said posted identifier at said associated local error indicator and starts said timer to time a predetermined time-out period; and responds to expiration of said time-out period of said timer, deleting said posted identifier from said local error indicator in column 15, lines 15-41.

16. As per claim 15, Jardine et al. discloses additionally comprising an operator input; and wherein at least one of said plurality of processor nodes, additionally, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and responds to an operator initiated signal at said operator input, deleting said posted identifier from said associated local error indicator in column 15, lines 15-41. The operator initiated signal is when the regroup message is sent.

17. As per claim 16, Jardine et al. discloses wherein at least one of said plurality of processor nodes additionally, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and said displaying processor node retesting said access, and, upon absence of an error during a predetermined number of said retests, deleting said posted identifier from said local error indicator in column 15, lines 10-41.

18. As per claim 17, Jardine et al. discloses additionally comprising multiple ones of said processor nodes extending from a single drop of said multi-drop bus network; wherein said information of relative locations of said plurality of processor nodes, additionally provides information of said processor nodes at said single drop; wherein each said failure detecting processor node additionally, upon detecting access failure of a plurality of said multiple processor nodes at said single drop, determines from said information of relative locations, said single drop having failed accesses which is closest to said failure detecting processor node, and selects one of said multiple processor nodes at said single

drop, said failure detecting processor node storing an identification of said selected processor node in column 13, line 46 – column 14, line 21; lines 45-67.

19. As per claim 18, Jardine et al. discloses wherein one of said multiple processor nodes extending from said single drop of said multi-drop bus network is identified in said information of relative locations as having a higher priority than other processor nodes extending from said single drop; and wherein each of said plurality of processor nodes additionally, upon detecting said access failure at said single drop, determines from said information of relative locations, said higher priority processor node, and selects and stores an identification of said multiple processor node having said higher priority in column 13, line 46 – column 14, line 21; lines 45-67.

20. As per claim 19, Jardine et al. discloses wherein said local error indicators comprise character displays of at least one character in column 13, line 46 – column 14, line 21.

21. As per claim 20, Jardine et al. discloses said distributed processing system comprising processor nodes coupled by a multi-drop bus network, said processor node comprising: an information table providing relative locations of said processor nodes on said multi-drop bus network; and a processor independently testing access to other said processor nodes on said multi-drop bus network; upon said access testing detecting a failure to access at least one of said other processor nodes, determining, from said information table of relative locations, the processor node having failed access which is closest to said failure

detecting processor node, and storing an identification of said closest processor node having failed access in column 13, line 46 – column 14, line 21; lines 45-67.

22. As per claim 21, Jardine et al. discloses additionally comprising a local error indicator associated with said processor of said failure detecting processor, said processor node posting, at said associated local error indicator, an identifier of said closest processor node having failed access in column 13, line 46 – column 14, line 2.

23. As per claim 22, Jardine et al. discloses additionally, upon said access testing detecting a failure to access all of said other processor nodes, said failure detecting processor n de posting a special identifier at said associated local error indicator in column 22, lines 52-56.

24. As per claim 23, Jardine et al. discloses additionally comprising an error log, and wherein said processor, upon detecting said access failure, posts an error message representing said identifier to said error log in column 13, line 46 – column 14, line 2.

25. As per claim 24, Jardine et al. discloses additionally comprising a timer; and wherein said processor, upon detecting said access failure, locks said posted identifier at said associated local error indicator and starts said timer to time a predetermined time-out period; and responds to expiration of said time-out period of said timer, deleting said posted identifier from said associated local error indicator in column 15, lines 15-41.

26. As per claim 25, Jardine et al. discloses additionally, upon detecting said access failure, locks said posted identifier at said associated local error indicator;

and responds to an operator initiated signal at an operator input, deleting said posted identifier from said associated local error indicator in column 15, lines 15-41. The operator initiated signal is when the regroup message is sent.

27. As per claim 26, Jardine et al. discloses said processor, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and retests said access, and, upon absence of an error during a predetermined number of said retests, deleting said posted identifier from said associated local error indicator in column 15, lines 10-41.

28. As per claim 27, Jardine et al. discloses wherein said multi-drop bus network comprises multiple processor nodes extending from a single drop of said multi-drop bus network; wherein said information table of relative locations of said processor node additionally provides said processor nodes at said single drop; wherein said processor additionally, upon detecting access failure of a plurality of said multiple processor nodes at said single drop, determines from said information table of relative locations, said single drop having failed access which is closest to said failure detecting processor node, selects one of said multiple processor nodes at said single drop, and stores an identification of said selected processor node in column 13, line 46 – column 14, line 21; lines 45-67.

29. As per claim 28, Jardine et al. discloses wherein one of said multiple processor nodes extending from said single drop of said multi-drop bus network is identified in said information table of relative locations as having a higher priority than other processor nodes extending from said single drop; and wherein said processor additionally, upon detecting said access failures at said single

drop, determines from said information table of relative locations, said higher priority processor node, and selects and stores an identification of said multiple processor node having said higher priority in column 13, line 46 – column 14, line 21; lines 45-67.

30. As per claim 29, Jardine et al. discloses wherein said associated local error indicator comprises a character display of at least one character in column 13, line 46 – column 14, line 21.

31. As per claim 30, Jardine et al. discloses for isolating failures of a multi-drop bus network in a distributed processing system, said distributed processing system comprising processor nodes coupled by said multi-drop bus network, comprising: computer readable program code which causes a computer processor of at least one of a plurality of said processor nodes to store information of relative locations of said processor nodes on said multi-drop bus network; computer readable program code which causes said computer processor to test, independently of other of said processor nodes, access to at least one other of said processor nodes on said multi-drop bus network; computer readable program code which causes said computer processor, upon said access testing detecting a failure to access at least one of said other processor nodes, to determine, from said provided information of relative locations, the processor node having failed access which is closest to said failure detecting processor node; and computer readable program code which causes said computer processor to store an identification of said closest processor node having failed access in column 13, line 46 – column 14, line 21; lines 45-67.

32. As per claim 31, Jardine et al. discloses additionally comprising computer readable program code which causes said computer processor to post, at a local error indicator associated with said failure detecting processor node, an identifier of said closest processor node having failed access in column 13, line 46 – column 14, line 2.

33. As per claim 32, Jardine et al. discloses additionally comprising computer readable program code which causes said computer processor, upon said access testing detecting a failure to access all of said other processor nodes, to post a special identifier at said associated local error indicator in column 22, lines 52-56.

34. As per claim 33, Jardine et al. discloses additionally comprising computer readable program code which causes said computer processor to provide an error log, and which causes said computer processor, upon detecting said access failure, to post an error message representing said identifier to said error log in column 13, line 46 – column 14, line 2.

35. As per claim 34, Jardine et al. discloses additionally comprising computer readable program code which causes said computer processor to provide a timer, and which causes said computer processor, upon detecting said access failure, to lock said posted identifier at said associated local error indicator and start said timer to time a predetermined time-out period, and to respond to expiration of said time-out period of said timer, deleting said posted identifier from said associated local error indicator in column 15, lines 15-41.

36. As per claim 35, Jardine et al. discloses wherein said computer readable program code additionally causes said computer processor, upon detecting said access failure, to lock said posted identifier at said associated local error indicator, and to respond to an operator initiated signal at an operator input, deleting said posted identifier from said associated local error indicator in column 15, lines 15-41. The operator initiated signal is when the regroup message is sent.

37. As per claim 36, Jardine et al. discloses wherein said computer readable program code additionally causes said computer processor, upon detecting said access failure, to lock said posted identifier at said associated local error indicator, and to retest said access, and upon absence of an error during a predetermined number of said retests, to delete said posted identifier from said associated local error indicator in column 15, lines 10-41.

38. As per claim 37, Jardine et al. discloses wherein said multi-drop bus network comprises multiple processor nodes extending from a single drop of said multi-drop bus network; and wherein said computer readable program code additionally causes said computer processor to provide said information of relative locations of said processor nodes to additionally provide information of said processor nodes at said single drop; and wherein said computer readable program code additionally causes said computer processor, upon detecting access failure of a plurality of said multiple processor nodes at said single drop, to determine from said information of relative locations, said single drop having failed access which is closest to said failure detecting processor node, to select

one of said multiple processor nodes at said single drop, and to store an identification of said selected processor node in column 13, line 46 – column 14, line 21; lines 45-67.

39. As per claim 38, Jardine et al. discloses wherein said computer readable program code additionally causes said computer processor to identify, in said provided information of relative locations, one of said multiple processor nodes extending from said single drop of said multi-drop bus network as having a higher priority than other processor nodes extending from said single drop; and wherein said computer readable program code additionally causes said computer processor, upon detecting said access failures at said single drop, to determine from said information of relative locations, said higher priority processor node, and to select an identification of said multiple processor node having said higher priority in column 13, line 46 – column 14, line 21; lines 45-67.

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

41. Claims 39-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jardine et al. in view of Rockwell (USPN 6204992B1). As appears in claim 39, Jardine discloses a multi-drop bus network; at least one communication

processor node for receiving commands, and coupled to said multi-drop bus network to provide a communication link for said commands; each of said processor nodes having information of relative locations of processor nodes on said multi-drop bus network; said processor nodes each independently testing access to other said processor nodes on said multi-drop bus network; upon said access testing by any of said testing processor nodes detecting a failure to access at least one of said other processor nodes, said failure detecting processor node determining, from said information of relative locations, the processor node having failed access which is closest to said failure detecting processor node; and said failure detecting processor node storing an identification of said closest processor node having failed access.

Jardine fails to explicitly state a robot accessor having a gripper and servo motors for accessing said data storage cartridges, said robot accessor having at least one processor node coupled to said multi-drop bus network for operating said gripper and said servo motors in response to said linked commands.

Rockwell discloses this limitation in column 4, lines 25-35.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a robot accessor having a gripper and servo motors for accessing said data storage cartridges, said robot accessor having at least one processor node coupled to said multi-drop bus network for operating said gripper and said servo motors in response to said linked commands. A person of ordinary skill in the art would have been motivated to have a robot accessor having a gripper and servo motors for accessing said data

storage cartridges, said robot accessor having at least one processor node coupled to said multi-drop bus network for operating said gripper and said servo motors in response to said linked commands because a processor can access data stored in the data storage cartridges located in the data storage library. Rockwell discloses this reasoning in column 3, lines 26-36.

42. As per claim 40, Jardine et al. discloses additionally comprising a plurality of local error indicators, each uniquely associated with at least one of said processor nodes, and wherein said failure detecting processor node additionally posts, at said local error indicator associated with said failure detecting processor node, an identification of said closest processor node having failed access in column 13, line 46 – column 14, line 2.

43. As per claim 41, Jardine et al. discloses wherein said processor nodes, additionally, upon said access testing by any of said testing processor nodes detecting a failure to access all of said other processor nodes, said failure detecting processor node posting a special identifier at said associated local error indicator in column 22, lines 52-56.

44. As per claim 42, Jardine et al. discloses wherein each of said processor nodes additionally comprises an error log, and, upon detecting said access failure, posts an error message representing said identifier to said error log in column 13, line 46 – column 14, line 2.

45. As per claim 43, Jardine et al. discloses wherein at least one of said processor nodes additionally comprises a timer; and, upon detecting said access failure, locks said posted identifier at said associated local error indicator and

starts said timer to time a predetermined time-out period; and responds to expiration of said time-out period of said timer, deleting said posted identifier from said associated local error indicator in column 15, lines 15-41.

46. As per claim 44, Jardine et al. discloses additionally comprising an operator panel comprising an operator panel processor node and an operator input; and wherein at least one of said processor nodes, additionally, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and responds to an operator initiated signal at said operator input, deleting said posted identifier from said associated local error indicator in column 15, lines 15-41. The operator initiated signal is when the regroup message is sent.

47. As per claim 45, Jardine et al. discloses wherein at least one of said processor nodes additionally, upon detecting said access failure, locks said posted identifier at said associated local error indicator; and said displaying processor node retesting said access, and, upon absence of an error during a predetermined number of said retests, deleting said posted identifier from said associated local error indicator in column 15, lines 10-41.

48. As per claim 46, Jardine et al. discloses additionally comprising multiple ones of said processor nodes extending from a single drop of said multi-drop bus network; wherein said provided information of relative locations of said plurality of processor nodes additionally determining said processor nodes at said single drop; wherein each of said processor nodes additionally, upon detecting access failure of a plurality of said multiple processor nodes at said single drop,

determines from said information of relative locations, said single drop having failed access which is closest to said failure detecting processor node, and selects one of said multiple processor nodes at said single drop, said failure detecting processor node storing an identification of said selected processor node in column 13, line 46 – column 14, line 21; lines 45-67.

49. As per claim 47, Jardine et al. discloses wherein one of said multiple processor nodes extending from said single drop of said multi-drop bus network is identified in said provided information of relative locations as having a higher priority than other processor nodes extending from said single drop; and wherein each of said plurality of processor nodes additionally, upon detecting said access failures at said single drop, determines from said information of relative locations, said higher priority processor node, and selects and stores an identification of said multiple processor node having said higher priority in column 13, line 46 – column 14, line 21; lines 45-67.

50. As per claim 48, Jardine et al. discloses wherein said local error indicators comprise character displays of at least one character in column 13, line 46 – column 14, line 21.

51. As per claim 49, Jardine et al. fails to explicitly state additionally comprising a plurality of interconnected frames, each having a plurality of said storage shelves, at least one of said frames coupling said at least one robot accessor processor node with said multi-drop bus network, at least one of said frames coupling said at least one communication processor node with said multi-

drop bus network, said processor nodes in each of said frame comprising at least one said relative location.

Rockwell discloses this limitation in column 2, lines 57-60 and column 4, lines 25-35. The additional racks disclosed in column 2, lines 57-60 are the additional interconnected frames discloses in claim 49.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a plurality of interconnected frames, each having a plurality of said storage shelves, at least one of said frames coupling said at least one robot accessor processor node with said multi-drop bus network, at least one of said frames coupling said at least one communication processor node with said multi-drop bus network, said processor nodes in each of said frame comprising at least one said relative location. A person of ordinary skill in the art would have been motivated to have a plurality of interconnected frames, each having a plurality of said storage shelves, at least one of said frames coupling said at least one robot accessor processor node with said multi-drop bus network, at least one of said frames coupling said at least one communication processor node with said multi-drop bus network, said processor nodes in each of said frame comprising at least one said relative location because more data storage cartridges can be added to the racks to provide more data for storage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yolanda Wilson whose telephone number is (703) 305-3298. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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